Customization of Embedded Software of Ionosonde to Use it as Wind Profiler

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Abstract— Ionosonde is an embedded system developed by SAMEER (Society of Applied Microwave Electronics Engineering and Research) for the ionosphere profiling. It uses the basic principle of reflection of Electromagnetic wave transmitted vertically, by ionosphere. It applies digital signal processing to the received signal to analyze the signal to determine the ionosphere components for the communication and other research purposes. This paper suggests modification of embedded software for the utilization of Ionosonde hardware system for wind profiling purposes. More emphasis will be given to the IP and the related signal processing part.

Keywords— Bi-phase coding, CIC filter, coherent integration, IP, Pulse compression, etc

I. INTRODUCTION

Ionosphere is a part of earth's atmosphere extending from about 50 km to 500 km above the earth's surface. This layer is capable of reflecting radio waves send towards it back to the earth. Hence this layer is very important from the point of view of wireless communication. Ionosonde is a pulsed Doppler radar that transmits the electromagnetic wave in the range of 0.5 MHz to 20 MHz in the vertical direction. The signal is reflected back by the ionosphere due to irregularities in the refractive index. The reflected signal has some Doppler added to it, by analysing the Doppler characteristic of ionosphere can be determined [1].

Wind profiler radar is also a pulsed Doppler radar which also analyses the reflected electromagnetic signal to determine the wind velocity. Wind profiler system follows Bragg's principle according to which, an electromagnetic wave can be scattered by the particles having size half the wavelength of an incident electromagnetic wave. Irregularities exist in a size range of a few centimeters to many meters. Hence the frequency of the wind profiler is kept in the range of 30MHz -3000 MHz. Here the proposed system works at the frequency of 50 MHz. As the basic structure and signal processing of the both Ionosonde and Wind profiler is same, we can utilize the hardware of the Ionosonde to construct Wind profiler radar with few modifications. The paper discusses the signal processing done in the Ionosonde and the modification need to be done in the embedded hardware to utilize it as Wind profiler radar.

II. IONOSONDE SYSTEM

Ionosonde is a system developed by SAMEER to measure the components of ionosphere. The system is used mainly for communication and research purpose. It transmits an electromagnetic wave in the vertical direction, which gets reflected by the ionosphere due to nonlinearities in the refractive index of the ionosphere. The nonlinearities are caused due to the variation in the electron densities in the ionosphere. The received signal is analyzed in the frequency domain to determine the Doppler shift produced in the transmitted signal and hence variation in the electron density in the ionosphere [2].

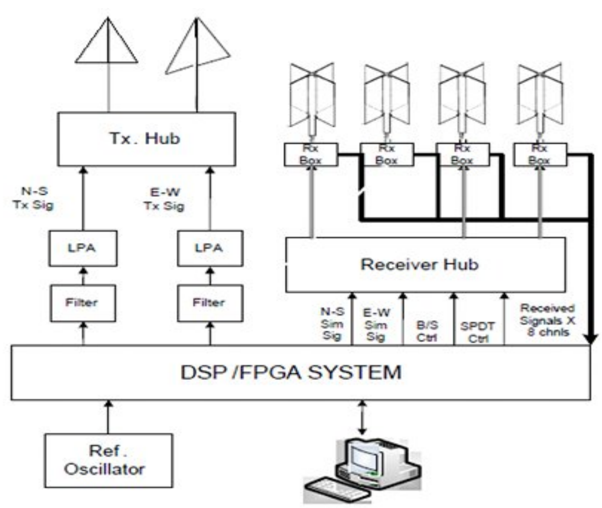

Fig.1 Ionosonde system overview

The system consists of three subsystems namely, transmitter system, Receiver system and Digital signal processing system. The digital signal processing system is implemented on implemented on FPGA.

A. Transmitter System

The transmitter system consists of RF antenna used for transmitting the encoded electromagnetic wave in the vertical direction. The system employs simple crossed delta or rhombic antenna for the transmission. The transmitted signal is complementary coded. Complementary coding is a pulse compression technique which enables high SNR at the low power of transmission. The encoding of the transmission signal is taken care by the FPGA system. The transmitted electromagnetic wave has frequency in the range of 0.5MHz to 20 MHz.

B. Receiver System

The receiver system is used for the reception of reflected electromagnetic wave. It consists of four crossed loop RF antenna. Each receiver has two channels that are utilized for the reception of two polarized signals separately. Receiver system also consists of data acquisition section which converts the analog signal into digital domain. The incoming RF signal between 0.5 MHz to 20 MHz is connected at ADC input. These signals must be sampled at high speed. The goal of this Data Acquisition component is to sample the ADC data at 60 Msps. The captured data from the ADCs is forwarded to the next module.

C. DSP/FPGA System

DSP system is the most important part of the Ionosonde. It takes care of the signal processing on the received signal. It also generates all the timing and control signal required for the operation of various components of the system. DSP/ FPGA system is divided into two parts. Namely, Signal processing unit and Mother board.

1) *Signal processing unit:* Ionosonde consists of four signal processing unit, also known as LAP board. The four LAP boards correspond to four channels used for the transmission of the electromagnetic signal. Each LAP board has two antenna input for two way polarized received signal. The LAP boards are implemented using four XC3S5000 FPGA boards, two high speed ADCs and parallel interface to communicate with mother board. IP cores available from library are used to implement various blocks on the FPGA. The main functions of signal processing boards are:

a) Digitizing the received signals using high speed ADC
b) Down converting the digitized signals.
c) Coherent integration to improve the SNR and to reduce the volume of data to be processed.
d) Transferring data to mother board using serial bus interface.

2) *Mother board:* Mother board generates all the timing and control signals required for the operation of parts of the system. Mother board consist Spartan-3A DSP 1800K gate FPGA, digital IOs, two DDS chips, RS232 and Ethernet MAC&PHY chips. Apart from these, there are 4 EURO connectors to interface with four LAP boards. The main functions of this Mother board are:

a) Clock distribution to the entire system
b) Timing and code signal generation
c) Generating bi-phase coded transmit signal using Direct Digital Synthesizer
d) Generating bi-phase coded simulated signal using DDS with programmable Doppler
e) Collecting data from 4 signal processing cards via bus interface.
f) Transferring data between the proposed system and PC through Ethernet and UART interfaces.

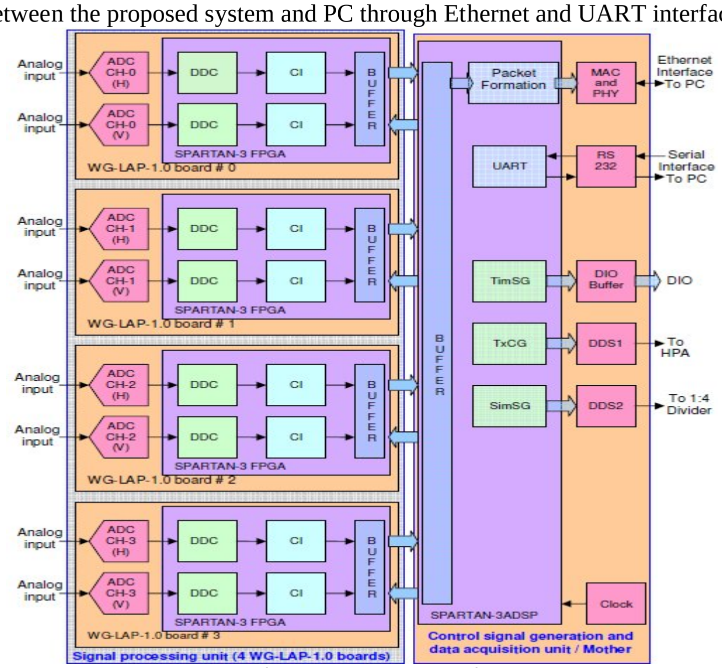

Fig.2 FPGA firmware block diagram of Ionosonde

III. SIGNAL PROCESSING

Ionosonde determines the ionosphere profile from the analysis of the back scattered electromagnetic waves. The electromagnetic wave is processed at the different stages for the number of purpose, Such as to achieve the improved signal to noise and resolution, to analyze the Doppler added to the transmitted signal, to simplify the hardware design, etc. The section describes the processes carried out on the electromagnetic waves.

A. Pulse compression

The signal transmitted by the transmitter system is complementary coded signal. Complementary coding is a pulse compression technique which enables the system to compensate low power transmitter. A way to increase the signal to noise ratio is to use pulses with more energy. The longer pulse allows a small low voltage solid state amplifier to transmit an amount of energy equal to that transmitted by a high power pulse transmitter (energy = power X time = V^2/R) without having to provide components to handle the high voltage required for tens of kilowatt power levels [3].

The radar range resolution for simple rectangular pulse waveform having the width of T is given by,

$$\Delta R = \frac{cT}{2} \quad \text{………………. (1)}$$

Range resolution can be improved by decreasing the pulse width of the transmitted signal.Hence it is desirable to have larger pulse width to achieve the low power transmission, but on the other hand smaller pulse width is desirable to achieve a better range resolution .To maintain the higher range resolution of the simple short pulse, the long pulse can be phase modulated with a code to enable the receiver to create a synthetic pulse with the short pulse. Ionosonde employs the Bi-phase code for the phase modulation. They let the RF carrier assume only two values for the phase: 0° and 180° with respect to a reference, following a pattern designed in order to achieve the low side lobes. The transmitted carrier wave is encoded before transmission and it is decoded after the reception. Encoding and decoding of the carrier wave is taken care by mother board implemented on FPGA.

B. Analog to digital conversion

The incoming RF signal between 1 MHz to 20 MHz is connected at ADC input. These signals must be sampled at high speed. There are two high speed ADCs available on each LAP board. The sampling rate for each ADC is 60 Msps. The goal of this Data Acquisition component is to sample the ADC data at 60 Msps. The captured data from the ADCs is forwarded to the next module.

C. Digital down conversion

The signal of interest in the sampled signal is of narrow bandwidth, the bandwidth of interest is only 33 KHz. Therefore the sampled data from the ADC is brought to baseband so as to use it for further processing. A DDC allows the frequency band of interest to be moved down the spectrum so the sample rate can be reduced. In this design the sampling rate at the input is 60 Msps which is down sampled to the 33 Ksps to achieve the required bandwidth of 33 KHz.

$$\text{Downsampling} = \frac{\text{Inputsamplingfrequency}}{\text{Outputsamplingfrequency}} = \frac{\text{60Msps}}{\text{33Ksps}} = 1800$$

DDC achieves the required down-sampling of 1800 in 3 stages. Stage1 achieves the down-sampling by30, stage 2 by 15 and stage 3 by 4. Stage 1 and stage 2 are CIC filters while stage 3 is a polyphase FIR filter. Polyphase FIR filter is used to compensate the magnitude response of CIC filter. CIC filters and polyphase filters are implemented using available IP cores [4].

D. Coherent Integration

In Ionosonde, Signal to noise ratio is increased by summing many echoes that allows the increasing the signal energy. When the signal echo is received, it carries information of various types; making some simplification we can represent each frequency component in the spectrum of the received signal with its phasor. Performing a valid integration on N pulses is equivalent to add many of these vectors with the same phase, yielding an amplitude N time greater [5]. The phasor of the noise has a random phase; the randomness of the phase is sufficient to cancel the noise. This technique is called as coherent integration. Coherent integration is done after receiving a reflected signal. Coherent Integration is handled by mother board using VHDL coding.

IV. TIMING AND CONTROL SIGNAL GENERATION

Timing and control signal generation (TCSG) module generates all timing and control signal. The module is implemented using IP core in microblaze processor. GUI on the PC is used to define the parameters of the transmitted signals. The microblaze receives the data packet containing different parameters from PC using Ethernet. The TCP/IP engine takes care of handling the Ethernet transfer. Microblaze extracts the required TCSG parameters from packet. A pCore is designed for the TCSG module such that once it is configured with different parameters, all timing signals will be generated as per requirement. The TCSG pCore communicates with microblaze via register bank. Microblaze writes the different parameters into register bank, pCore reads those parameters.

V. WORKING PRINCIPLE OF A WIND PROFILER

When a transmitted pulse encounters a target it is scattered in all directions. Out of the total scattered energy, the energy scattered in the direction opposite to the direction of transmission is received by the RADAR. This signal is much weaker than transmitted wave and called as back-scattered wave. Scattering of the electromagnetic wave follows the Bragg's principle. Bragg's principle states that, an electromagnetic wave can be scattered by the particles having size half the wavelength of an incident electromagnetic wave. Irregularities exist in a size range of a few centimeters to many meters. For wind profiling radars, frequency rang e of 30-3000 MHz (i.e., VHF and UHF bands) is generally used. Wind profiling radars operated at approximately 50 MHz frequency are not sensitive for small-sized cloud particles. Therefore 50-MHz wind profiling radars are able to measure vertical and horizontal wind velocities in both the clear air and cloudy regions [6] [7].

VI. MODIFICATION OF THE EMBEDDED SOFTWARE

Wind profiler can be developed using the same hardware of the Ionosonde. Due to change in the frequency and the parameters to be calculated, the changes need to be in the hardware, software and signal processing. The changes are proposed further.

A. Hardware changes in the LAP boards

The Ionosonde works at the frequency within the range of 0.5 MHz – 20 MHz. The sampling frequency of 50 MHz can be used for the digitization of the received signal. In the wind profiler the range of the frequency changes to 0.5 MHz – 50 MHz, hence the sampling frequency has to be greater than 100 MHz. The ADCs on the LAP board are of 60 Msps, hence these needs to be replaced with the ADCs with the higher sampling frequency. Ionosonde employs LT2205 for the analog to digital conversion. The proposed system can use LT2207 with the sampling frequency of 105 Msps.

B. Digital Down Conversion

In the Ionosonde system the sampling frequency of 60 Msps is brought to 33 Ksps by performing the decimation of 1800. The signal with the sampling frequency of 105 Msps needs to be decimated by 3100 approximately to bring it to the baseband. As,

$$\frac{105\text{Msps}}{33\text{Ksps}} \approx 3180$$

The required decimation can be achieved in the three steps as in Ionosonde. Two CIC filters carry out decimation of 31 and 25 respectively. Polyphase FIR filter which is used for compensating the magnitude response of CIC filter carry out decimation of 4.

C. Clock Signal

All the hardware components, microblaze processor and the peripherals implemented using IP core are synchronized using a clock signal. The clock signal is generated using Digital Clock Manager (DCM). DCM is implemented on motherboard using an IP core. In Ionosonde it generates the clock of frequency of 60 MHz, whereas in the wind profiler it generates the clock of the frequency 105 MHz.

D. Timing and control signal

Ionosonde uses a customized IP core which generates the required timing and control signals. With the change in the Pulse Width Duration (PWD), Inter Pulse period (IPP), etc. the IP core also needs to be modified.

Signal processing carried out in the PC will also change as different parameters need to be extracted from the wind profiler than Ionosonde. But the discussion is out of the scope of the paper.

VII. SIMULATION RESULTS

Simulation results for the timing and control signal generation with the following parameters:
Clock frequency = 105 MHz   Pulse Width Duration = 80 us   Inter Pulse Period = 1 ms.

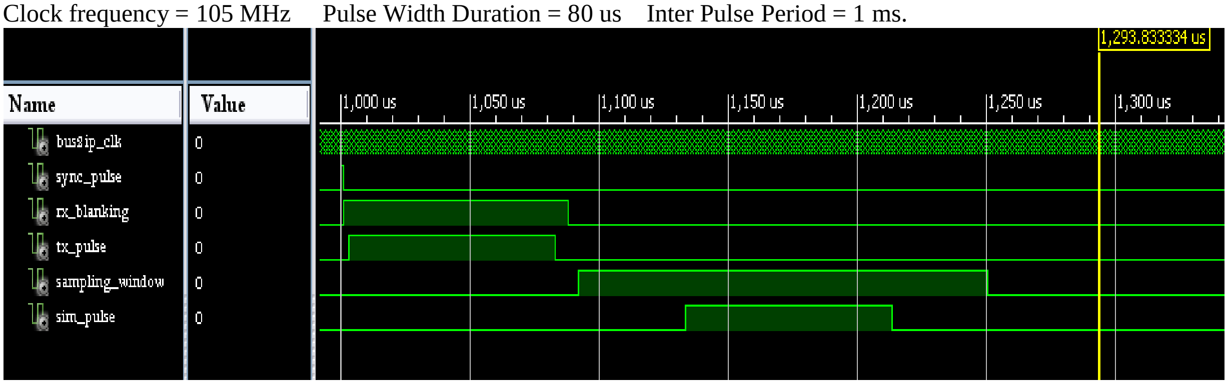

Fig.3 Timing and control signal generated by the TCSG core

VIII. CONCLUSIONS

Embedded software of the Ionosonde has been modified to change the processing of the received signal and the timing and control signals required for controlling operation of all hardware and software components. The simulation results show the changes in the timing and control signal. Operating the system in the simulation mode shows desired signals to the input of the PC. These signals can be further process to extract the desired wind speed parameters.

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